Integrated System-Level Modeling of Network-on-Chip enabled Multi-Processor Platforms

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The drastic performance, flexibility and energy-efficiency requirements of embedded applications drive the System-on-Chip integration towards heterogeneous multiprocessor platforms. Electronic System Level (ESL) design methodologies and tools have emerged to tackle the challenges of such complex SoC designs prior to RTL and silicon availability. In particular SystemC based Transaction Level Modeling (TLM) has matured as a standards-based approach to model SoC platforms for the purpose of Software development, system integration and verification.

In response to the vast complexity of heterogeneous multi-processor platforms the 'Architects View' is emerging as a new TLM use-case to address the architecture definition and application mapping by means of timing approximate transaction-level models. Integrated System-Level Modeling of Network-on-Chip Enabled Multi-Processor Platforms first gives a comprehensive update on recent developments in the area of SoC platforms and ESL design methodologies. The main contribution is the rigorous definition of a framework for modeling at the timing approximate level of abstraction. Subsequently this book presents a set of tools for the creation and exploration of timing approximate SoC platform models.

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